Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An electrostatic discharge (ESD) protection device, comprising:
an ESD clamp circuit, comprising:
at least a diode connected in series between a first voltage and a pad; and
at least an ESD component connected in series between a second voltage and a pad, wherein each of the at least an ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.

[c2] 2. The ESD protection device of claim 1, wherein when a number of the ESD component is one, the N+ region of the ESD component is connected to the pad, and the P+ region of the ESD component is connected to the second voltage.

[c3] 3. The ESD protection device of claim 1, wherein when a number of the ESD component is two including a 1^{st} ESD component and a 2^{nd} ESD component, the N+ region of a 1^{st} ESD component is connected to the pad, the P+ re-

gion of the 2nd ESD component is connected to the second voltage, and the P+ region of the 1st ESD component is connected to the N+ region of the 2nd ESD component.

[c4] 4. The ESD protection device of claim 1, wherein when a number of the ESD component is S including a 1st ESD component to a Sth ESD component, the N+ region of the 1st ESD component is connected to the pad, the P+ region of the Sth ESD component is connected to the second voltage, and the P+ region of the Tth ESD component is connected to the N+ region of the (T+1)th ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[c5] 5. The ESD protection device of claim 1, wherein each of the at least a diode comprises a N-well region formed in a P-type substrate, and a N+ region and a P+ region formed in the N-well region.

[c6] 6. The ESD protection device of claim 1, wherein when a number of the diode is one, the N+ region of the diode is connected to the first voltage, and the P+ region of the diode is connected to the pad.

[c7] 7. The ESD protection device of claim 1, wherein when a number of the diode is two including a first diode and a second diode, the N+ region of a first diode is connected

to the first voltage, the P+ region of the second diode is connected to the pad, and the P+ region of the first diode is connected to the N+ region of the second diode.

[c8] 8. The ESD protection device of claim 1, wherein when a number of the diode is S including a 1^{st} diode to a S^{th} diode, the N+ region of the 1^{st} diode is connected to the first voltage, the P+ region of the S^{th} diode is connected to the pad, and the P+ region of the T^{th} diode is connected to the N+ region of the $(T+1)^{th}$ diode, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[c9] 9. The ESD protection device of claim 1, wherein the ESD protection circuit further comprises another ESD clamp circuit comprising:
a PMOS transistor; and
an NMOS transistor, wherein a gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to a drain of the NMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage.

[c10] 10. The ESD protection device of claim 1, wherein the ESD protection device is a radio frequency (RF) ESD protection device.

[c11] 11. An electrostatic discharge (ESD) protection device, comprising:
an ESD clamp circuit, comprising:
at least a first ESD component connected in series between a first voltage and a pad; and
at least a second ESD component connected in series between a second voltage and a pad, wherein each of the at least a first ESD component or the at least a first ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.

[c12] 12. The ESD protection device of claim 11, wherein when a number of the first ESD component is one, the N+ region of the first ESD component is connected to the pad, and the P+ region of the first ESD component is connected to the second voltage.

[c13] 13. The ESD protection device of claim 11, wherein when a number of the first ESD component is two including a 1^{st} first ESD component and a 2^{nd} first ESD component, the N+ region of a 1^{st} first ESD component is connected to the pad, the P+ region of the 2^{nd} first ESD component is connected to the second voltage, and the P+ region of

the 1st first ESD component is connected to the N+ region of the 2nd first ESD component.

[c14] 14. The ESD protection device of claim 11, wherein when a number of the first ESD component is S including a 1st first ESD component to a Sth first ESD component, the N+ region of the 1st first ESD component is connected to the pad, the P+ region of the Sth first ESD component is connected to the second voltage, and the P+ region of the Tth first ESD component is connected to the N+ region of the (T+1)th first ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[c15] 15. The ESD protection device of claim 11, wherein when a number of the second ESD component is one, the N+ region of the second ESD component is connected to the first voltage, and the P+ region of the second ESD component is connected to the pad.

[c16] 16. The ESD protection device of claim 11, wherein when a number of the second ESD component is two including a 1st second ESD component and a 2nd second ESD component, the N+ region of a 1st second ESD component is connected to the first voltage, the P+ region of the 2nd second ESD component is connected to the pad, and the P+ region of the 1st second ESD component is connected to the N+ region of the 2nd second ESD component.

[c17] 17. The ESD protection device of claim 11, wherein when a number of the second ESD component is S including a 1^{st} second ESD component to a S^{th} second ESD component, the N+ region of the 1^{st} second ESD component is connected to the first voltage, the P+ region of the S^{th} second ESD component is connected to the pad, and the P+ region of the T^{th} second ESD component is connected to the N+ region of the $(T+1)^{th}$ second ESD component, wherein S is a positive integer and T is a positive integer from 1 to S-1.

[c18] 18. The ESD protection device of claim 11, wherein the ESD protection device is a radio frequency (RF) ESD protection device.

[c19] 19. The ESD protection device of claim 11, wherein the ESD protection circuit further comprises another ESD clamp circuit comprising:
a PMOS transistor; and
an NMOS transistor, wherein a gate of the PMOS transistor and a gate of the NMOS transistor are connected to the pad, a source of the PMOS transistor is connected to a drain of the NMOS transistor, a drain of the PMOS transistor is connected to the first voltage, and a source of the NMOS transistor is connected to the second voltage.